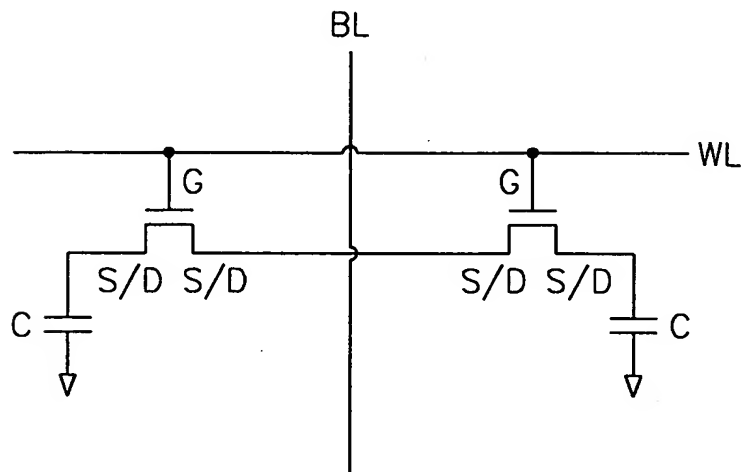


FIG. 1 (PRIOR ART)



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FIG. 2A (PRIOR ART)

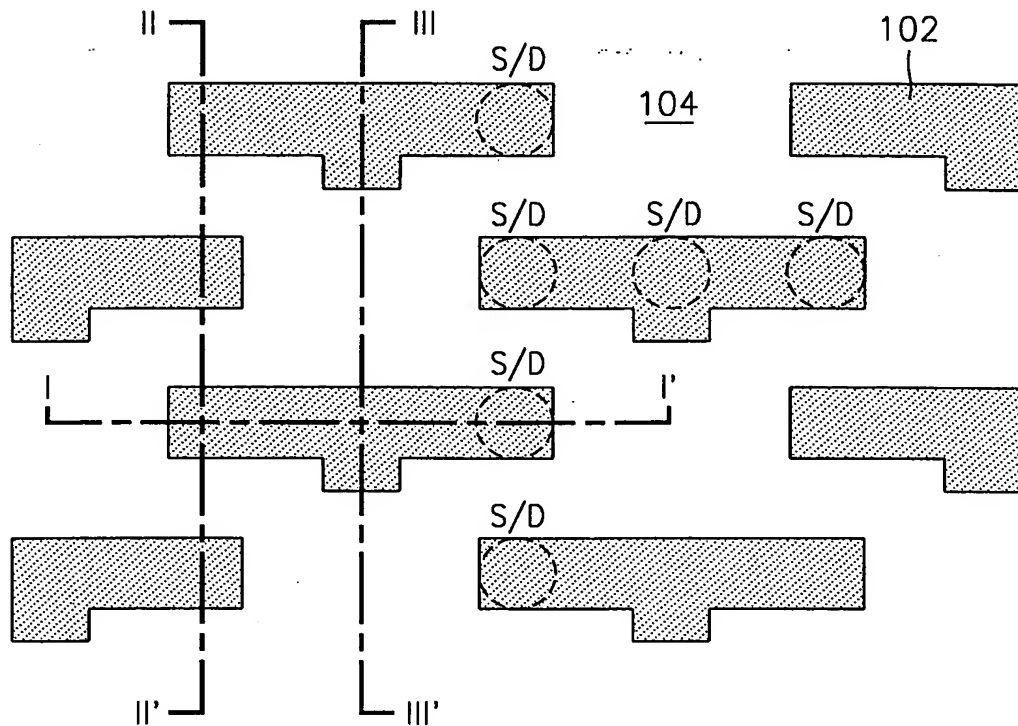


FIG. 2B (PRIOR ART)

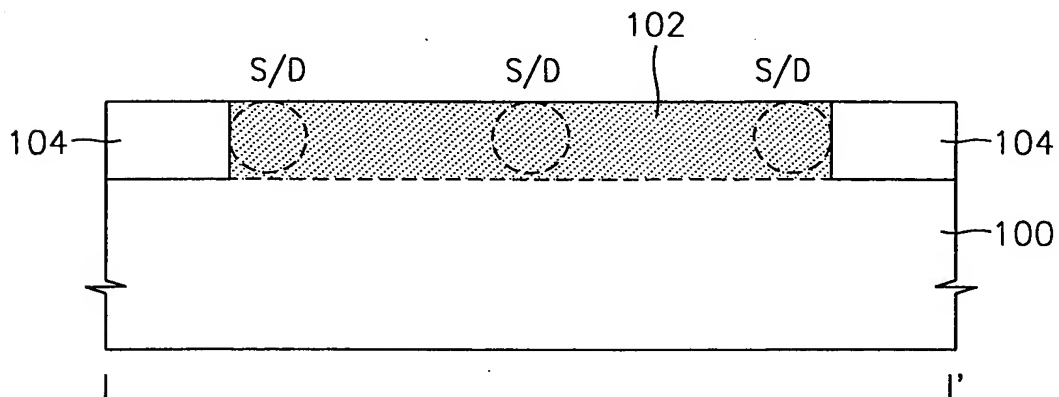


FIG. 2C (PRIOR ART)

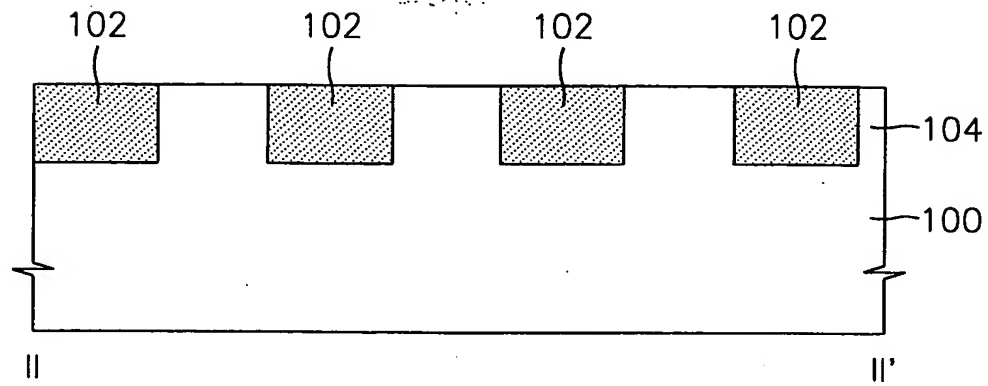
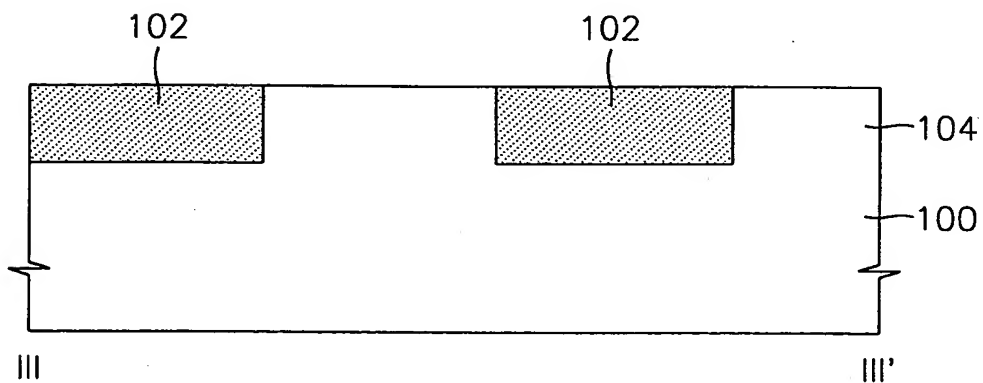


FIG. 2D (PRIOR ART)



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FIG. 3A (PRIOR ART)

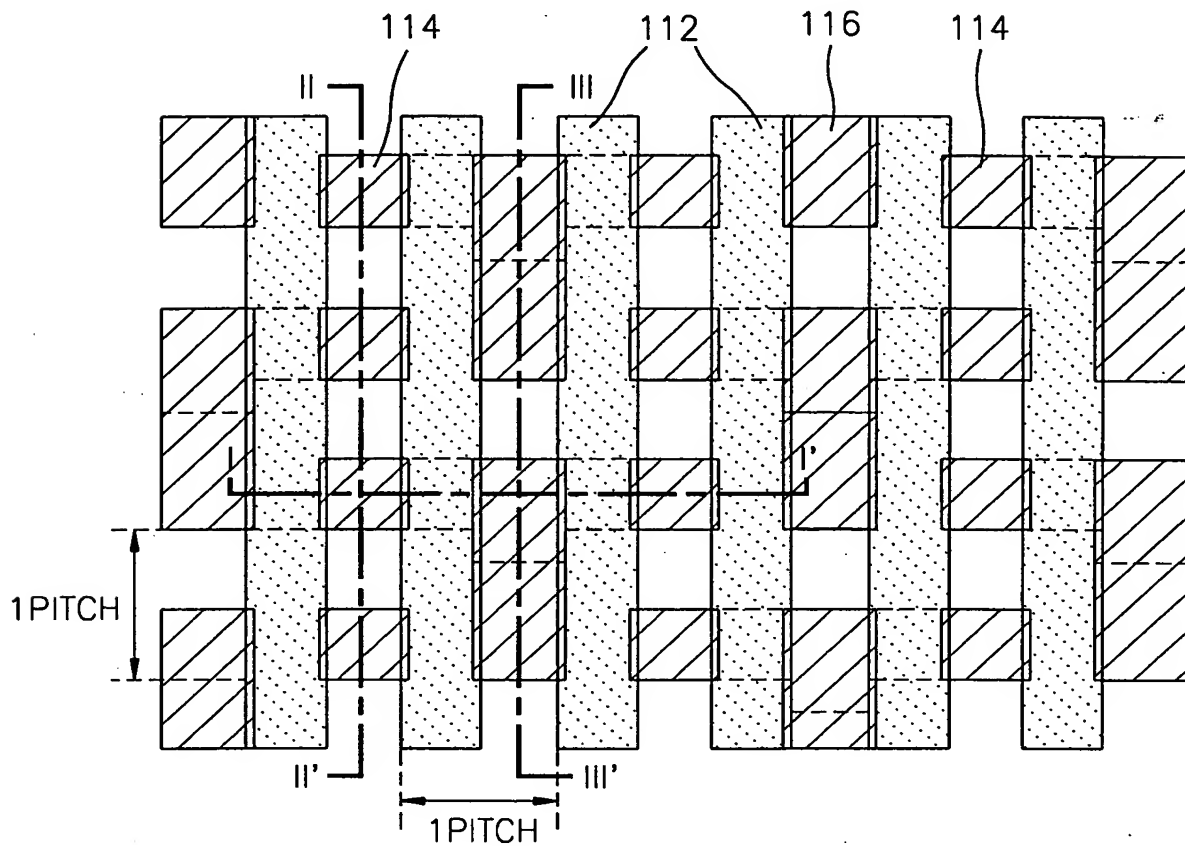
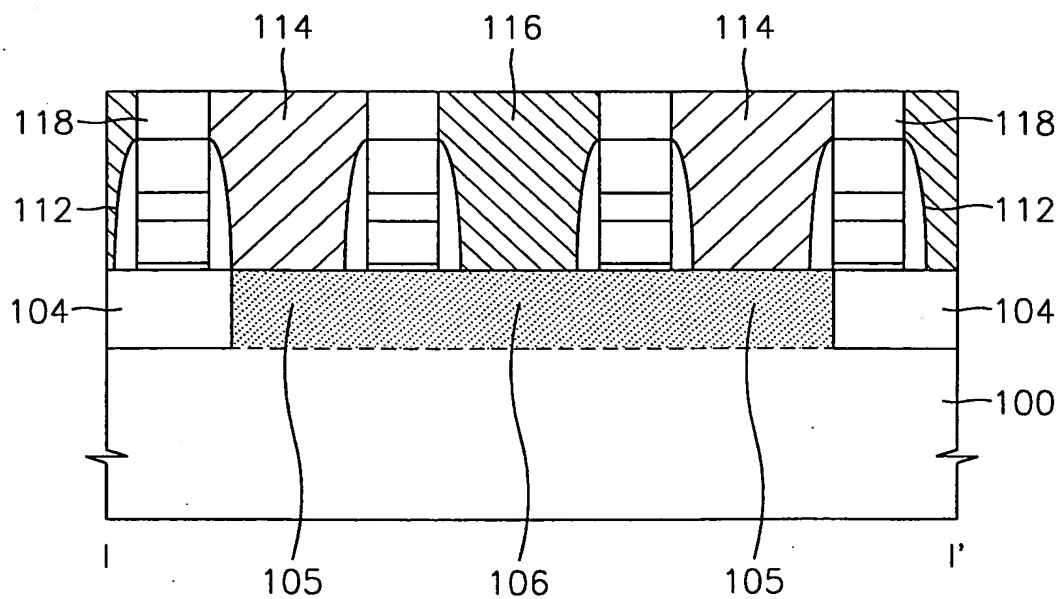


FIG. 3B (PRIOR ART)



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FIG. 3C (PRIOR ART)

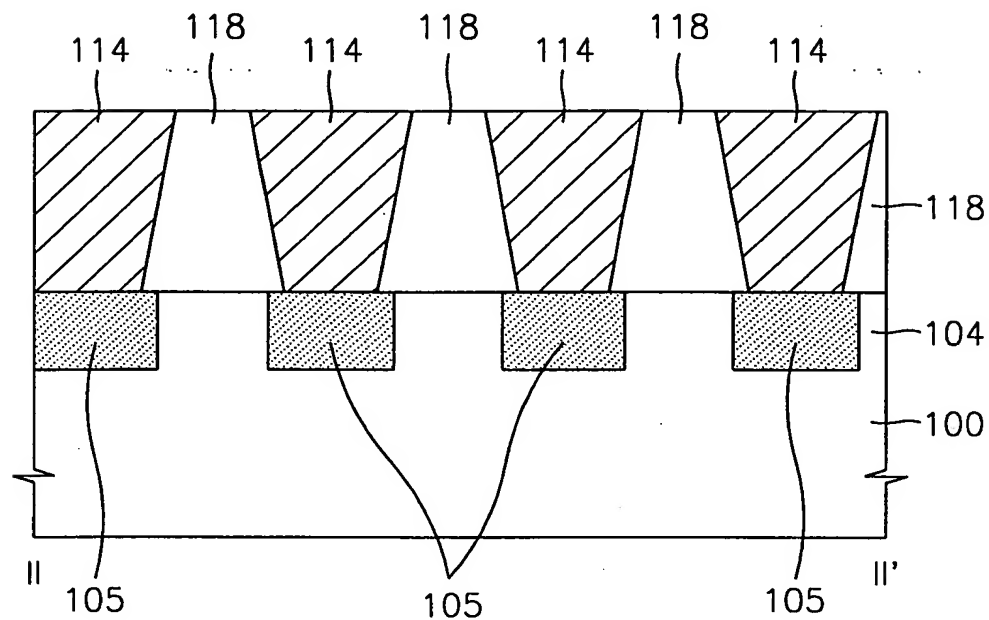
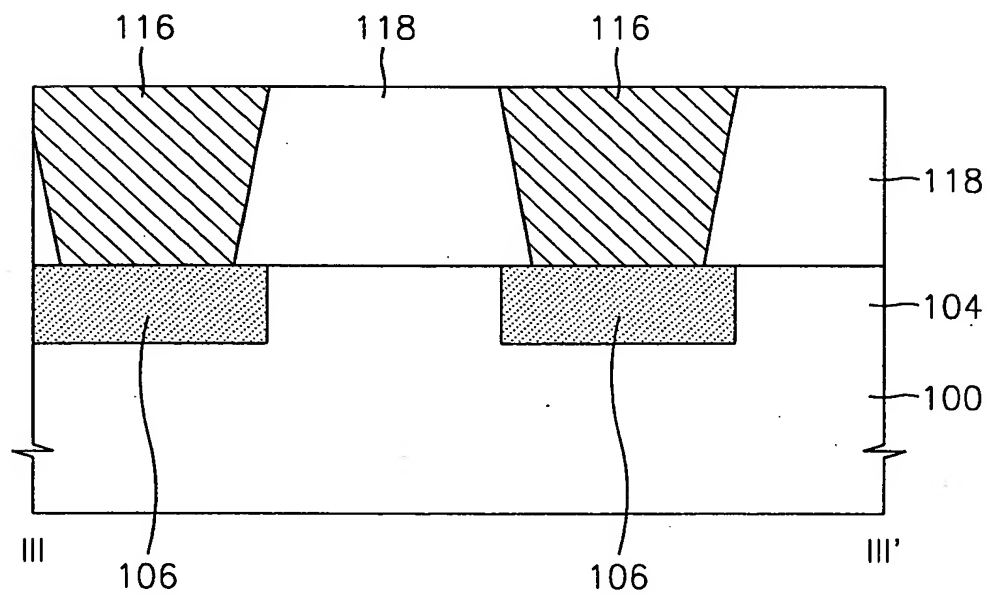


FIG. 3D (PRIOR ART)



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FIG. 4A (PRIOR ART)

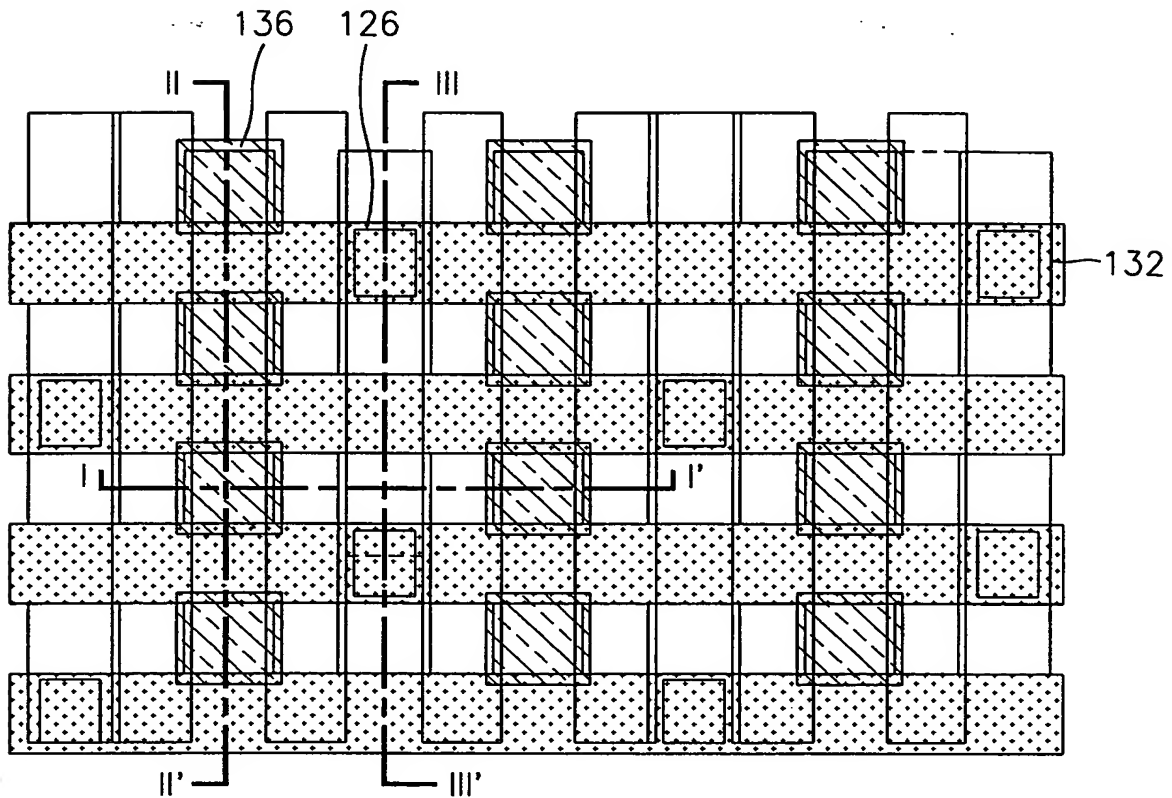


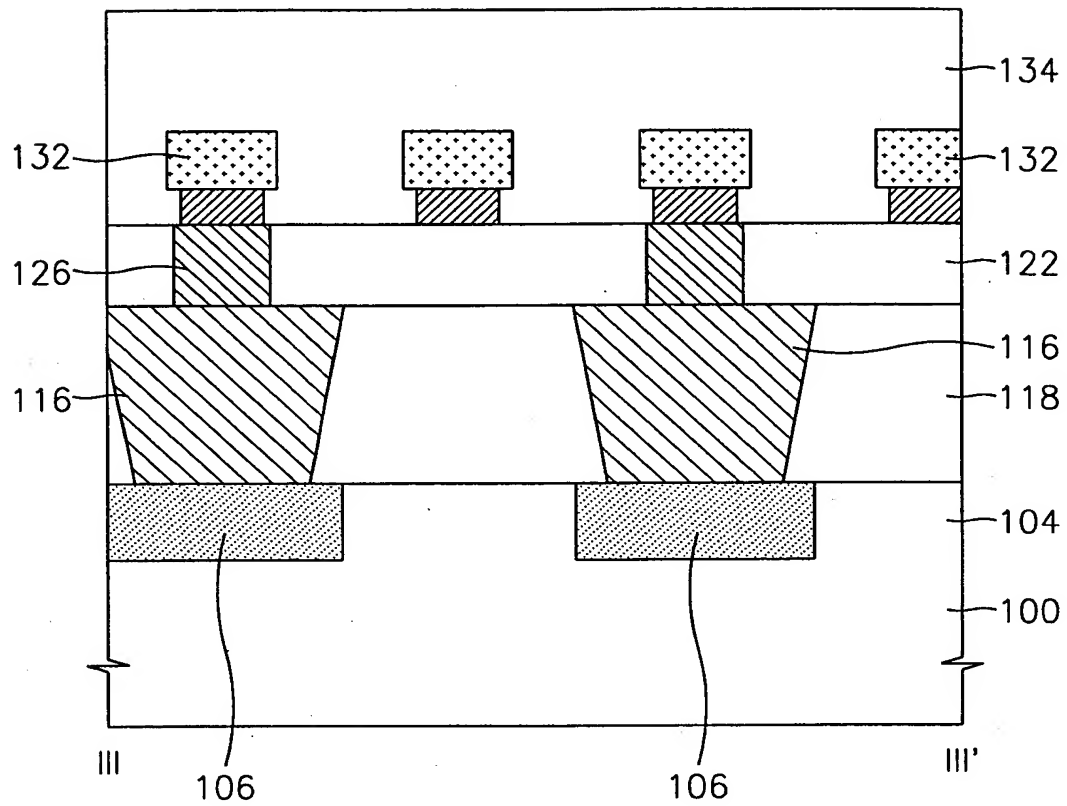
Fig. 1 is a cross-sectional view of a semiconductor device. The device includes a substrate 100. A layer 104 is formed on the substrate 100. A central region 114 is covered by a patterned layer 112, 116, 118. A layer 122 is above this, and a layer 134 is at the top. A layer 136 is on the sides, with 136a and 136b indicating different parts. A layer 106 is at the bottom of the central region.





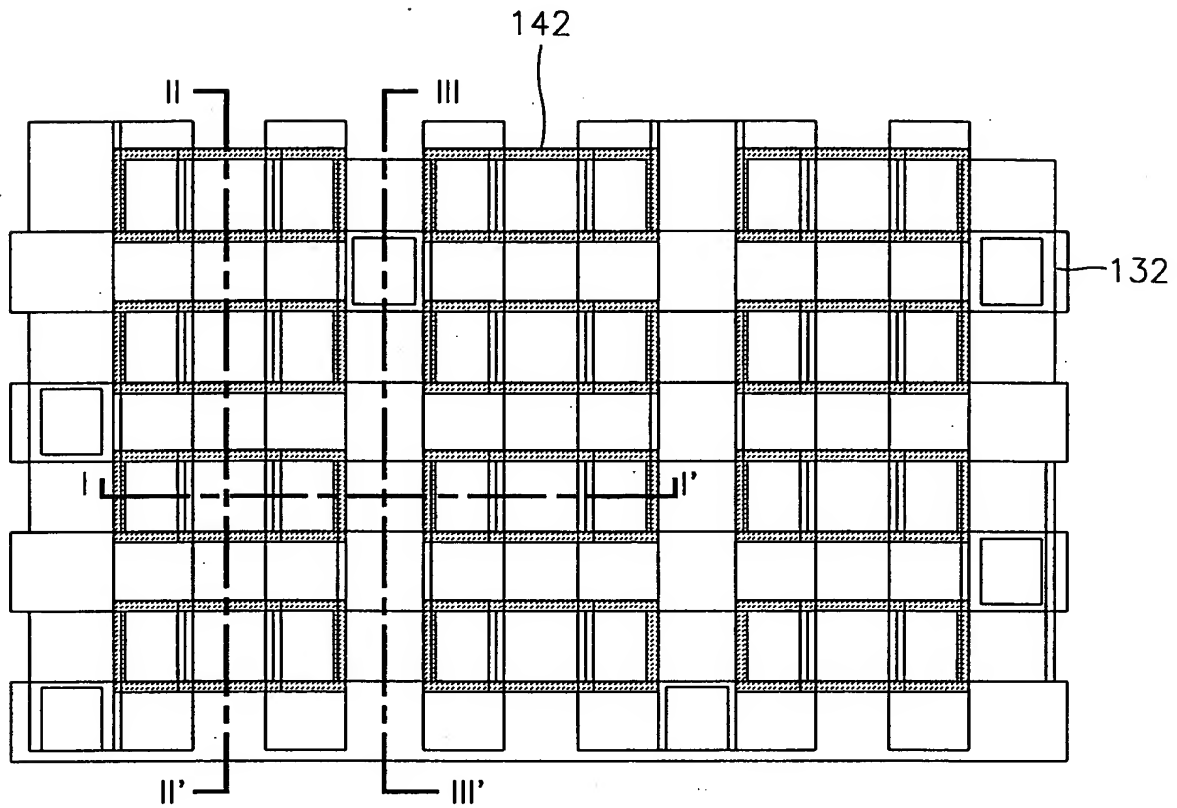
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FIG. 4D (PRIOR ART)



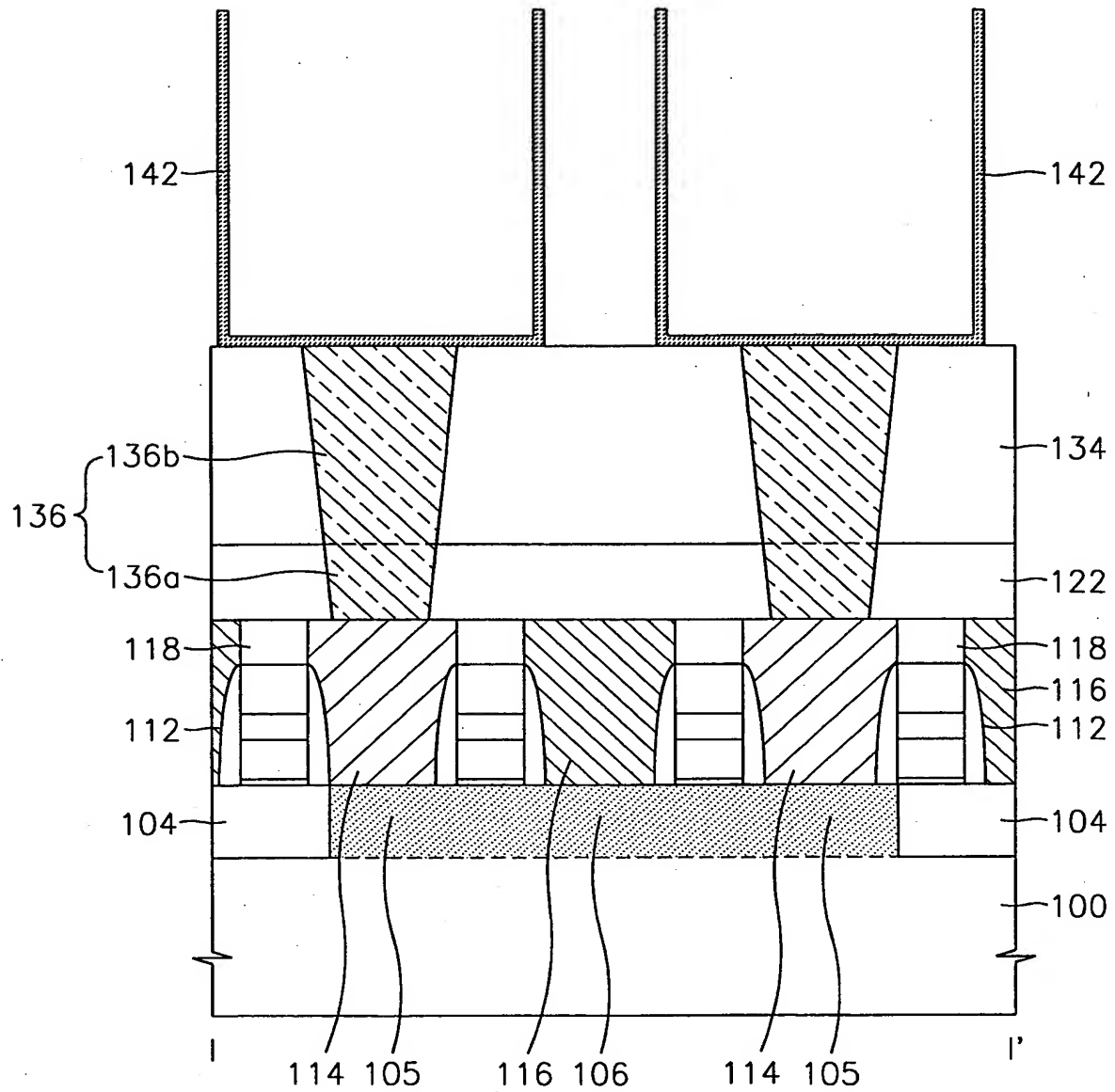
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FIG. 5A (PRIOR ART)



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FIG. 5B (PRIOR ART)



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FIG. 5C (PRIOR ART)

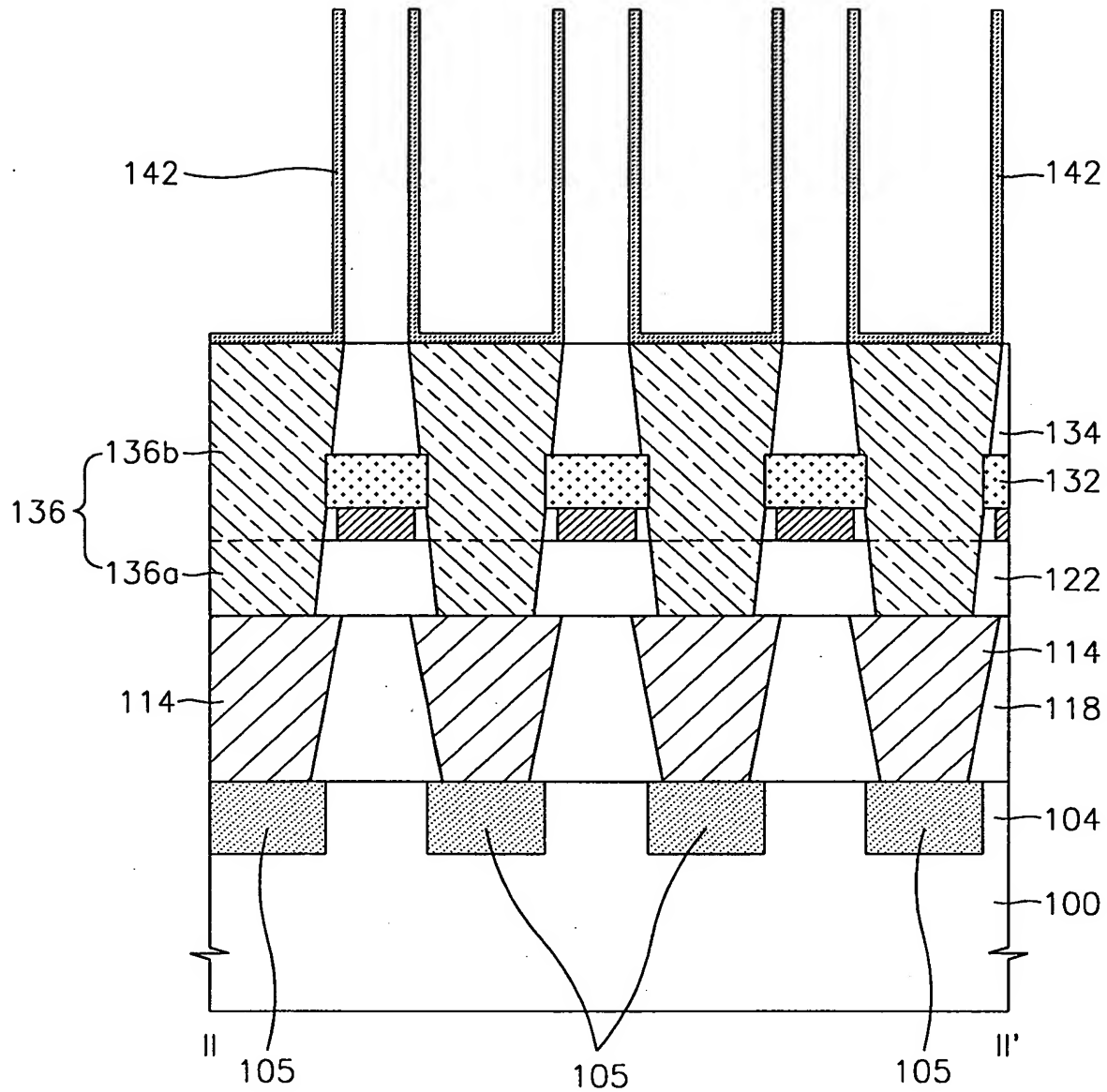
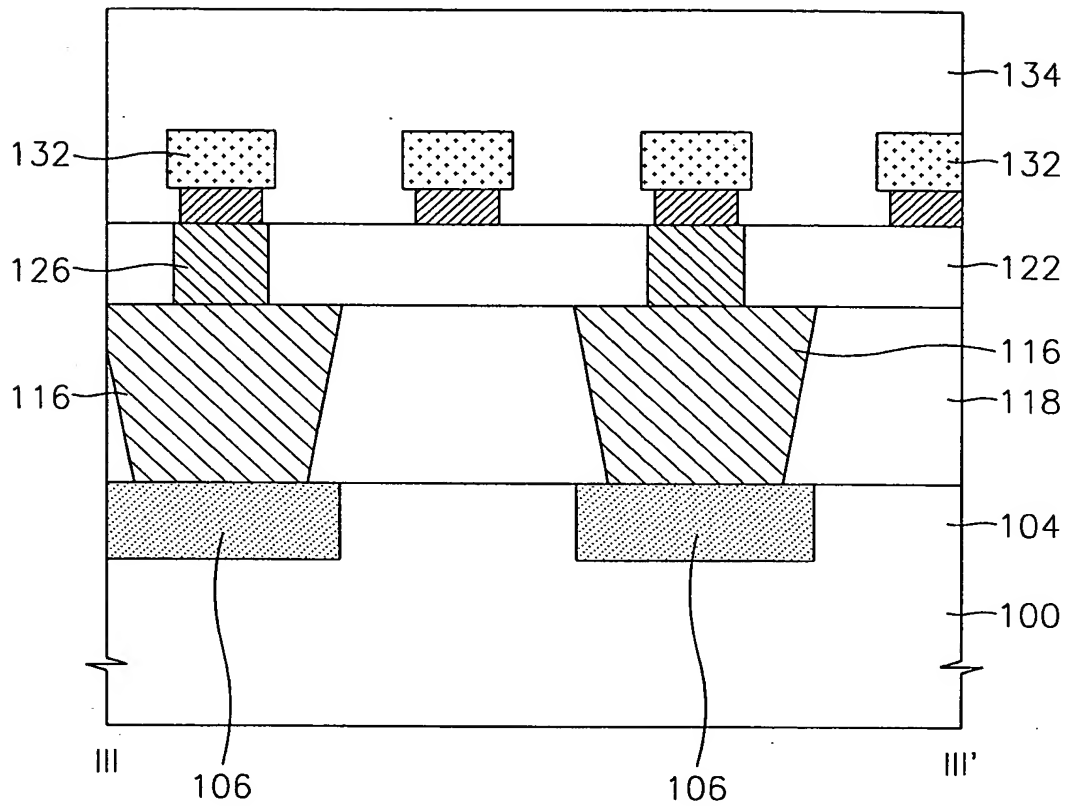


FIG. 5D (PRIOR ART)



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FIG. 6A

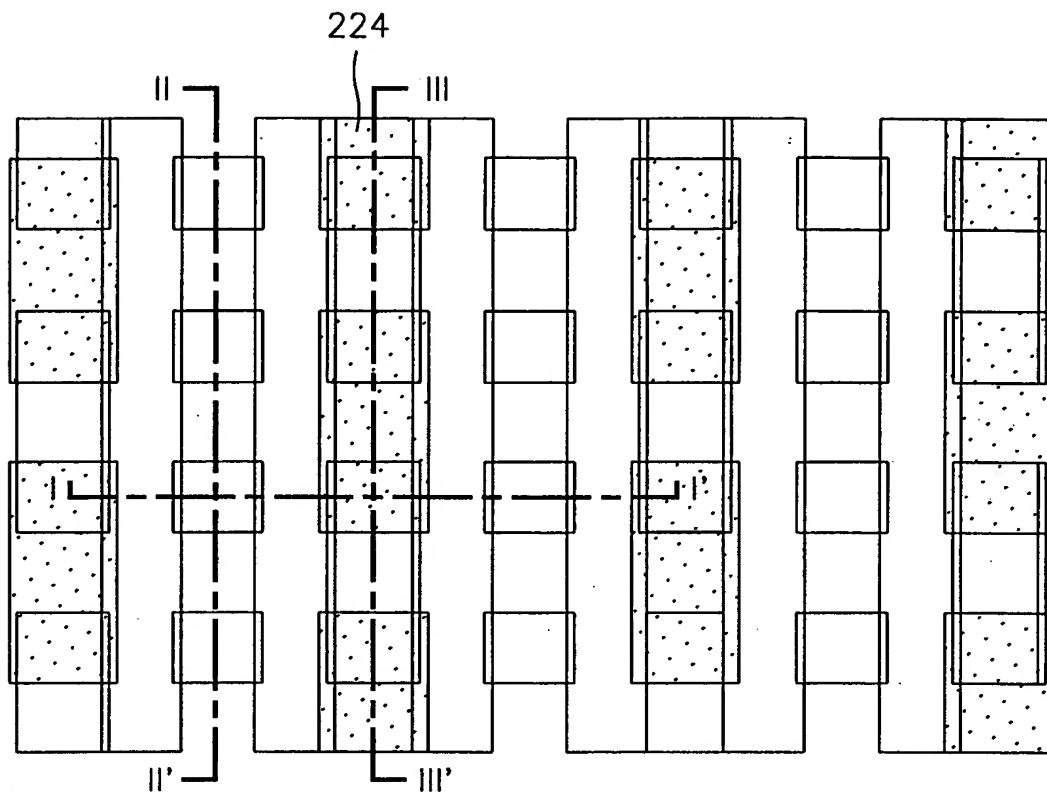
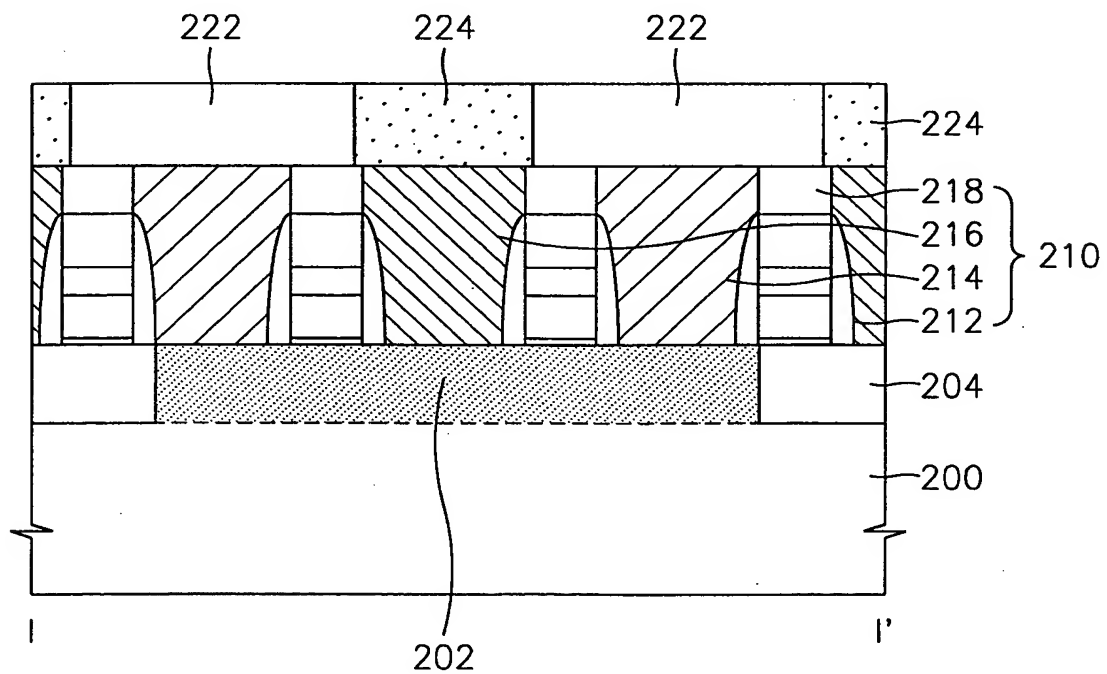


FIG. 6B



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FIG. 6C

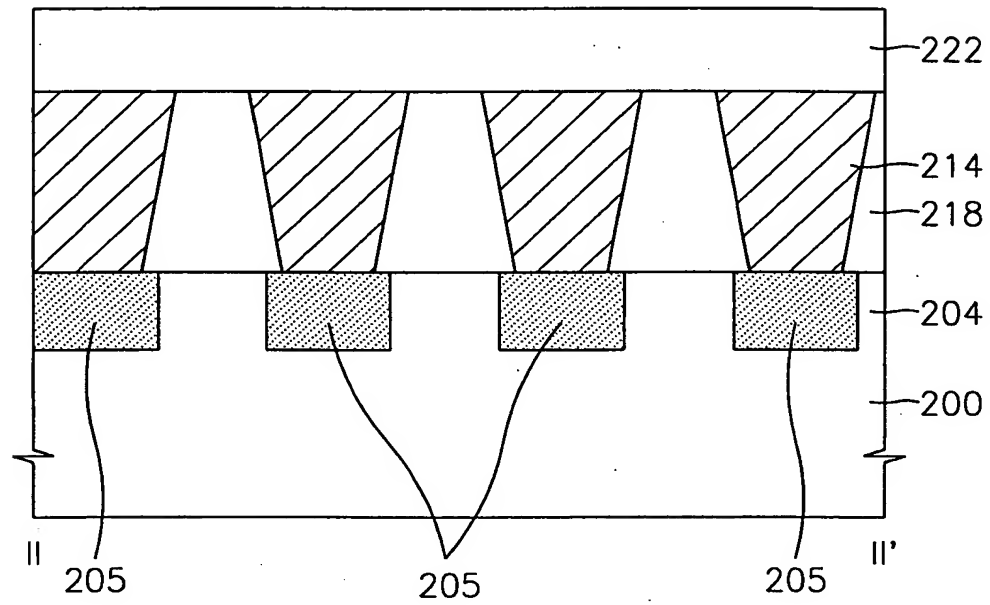
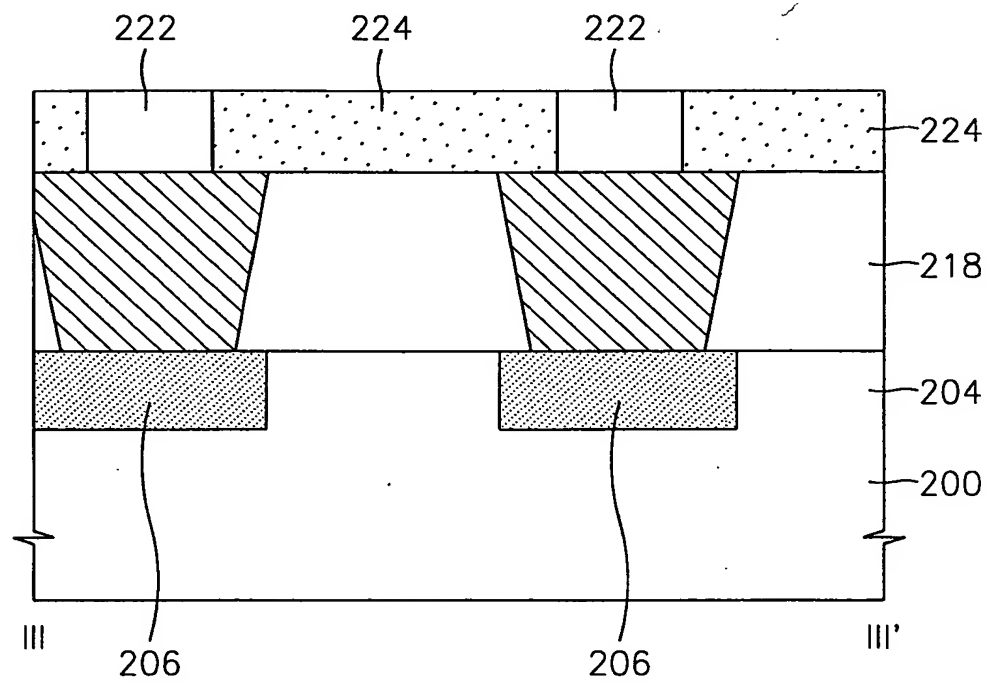


FIG. 6D



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FIG. 7A

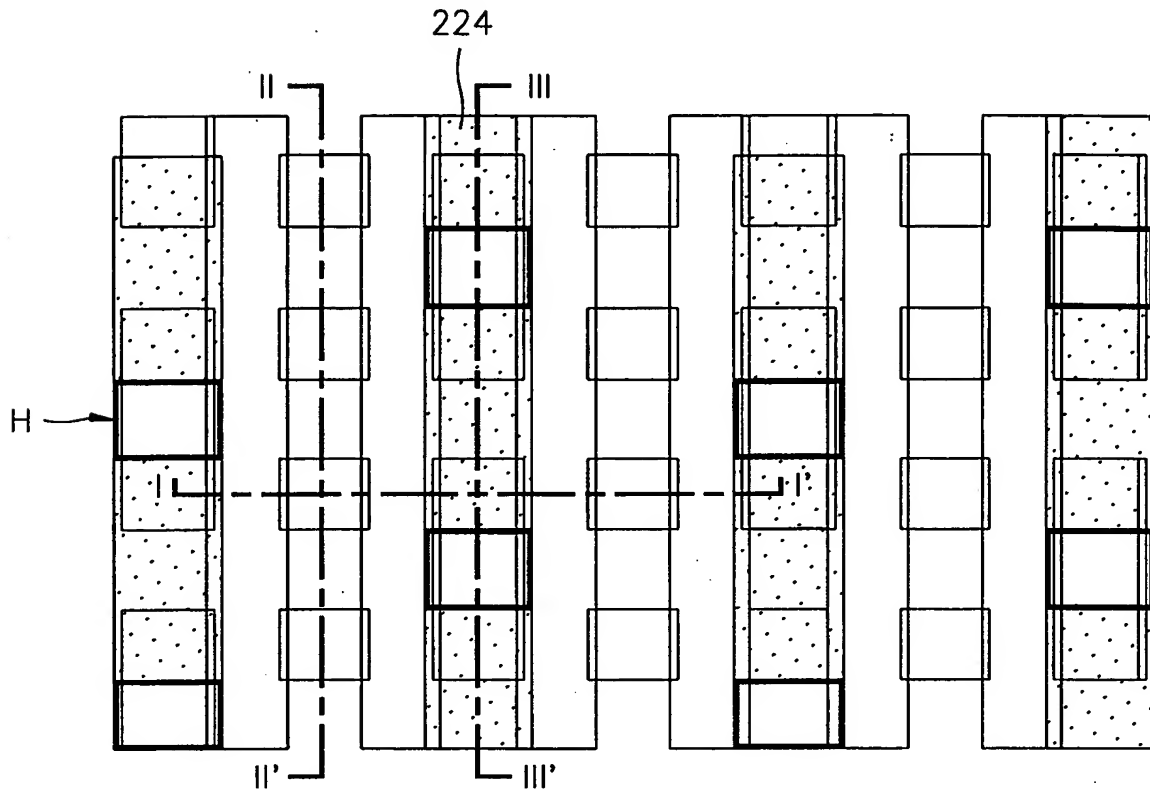
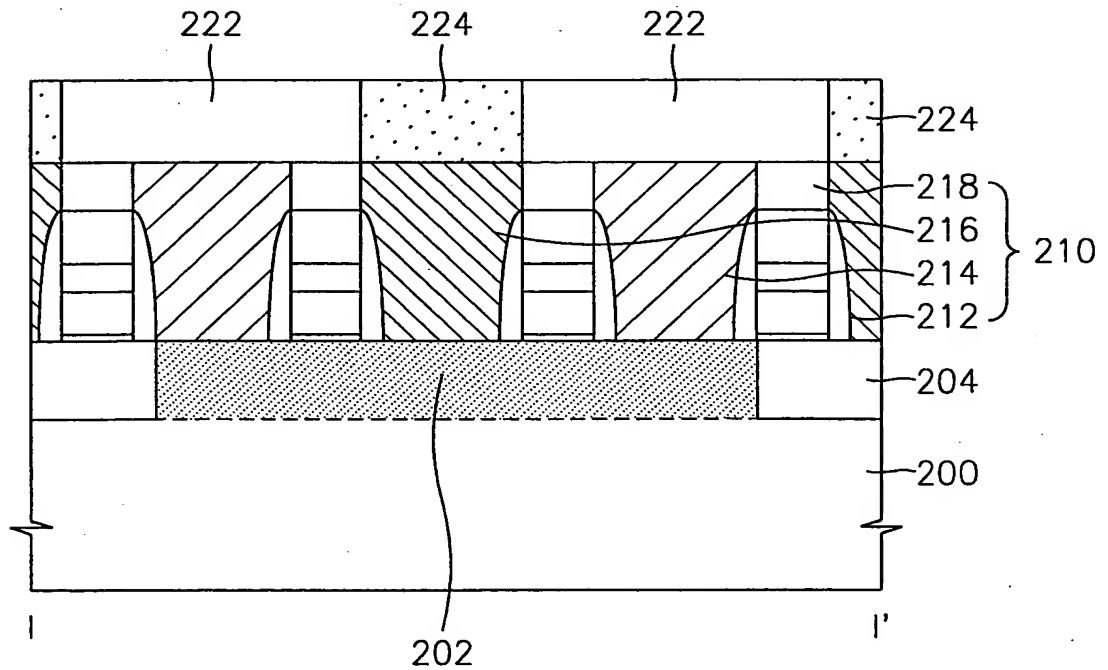


FIG. 7B





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FIG. 7C

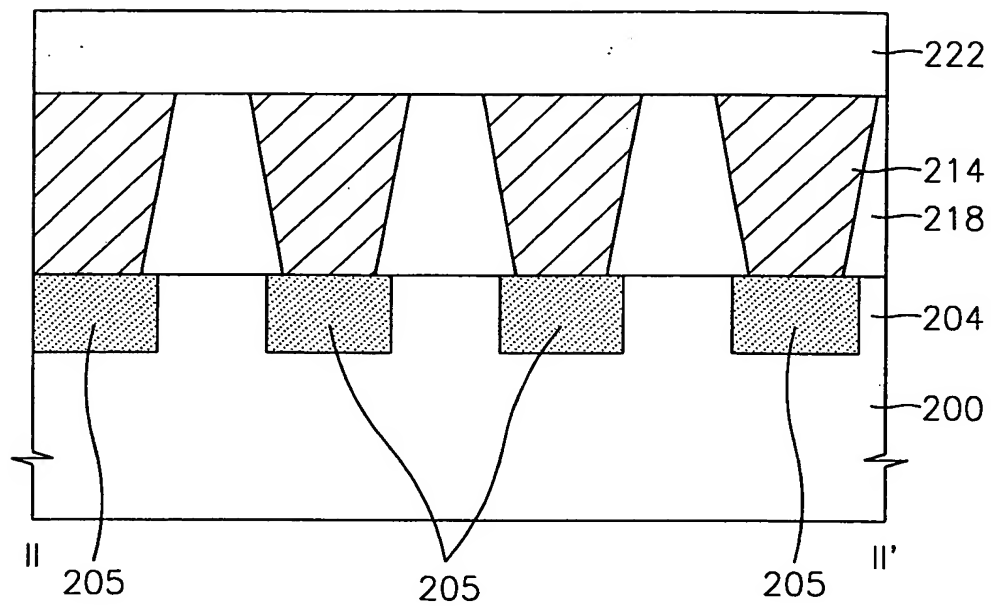
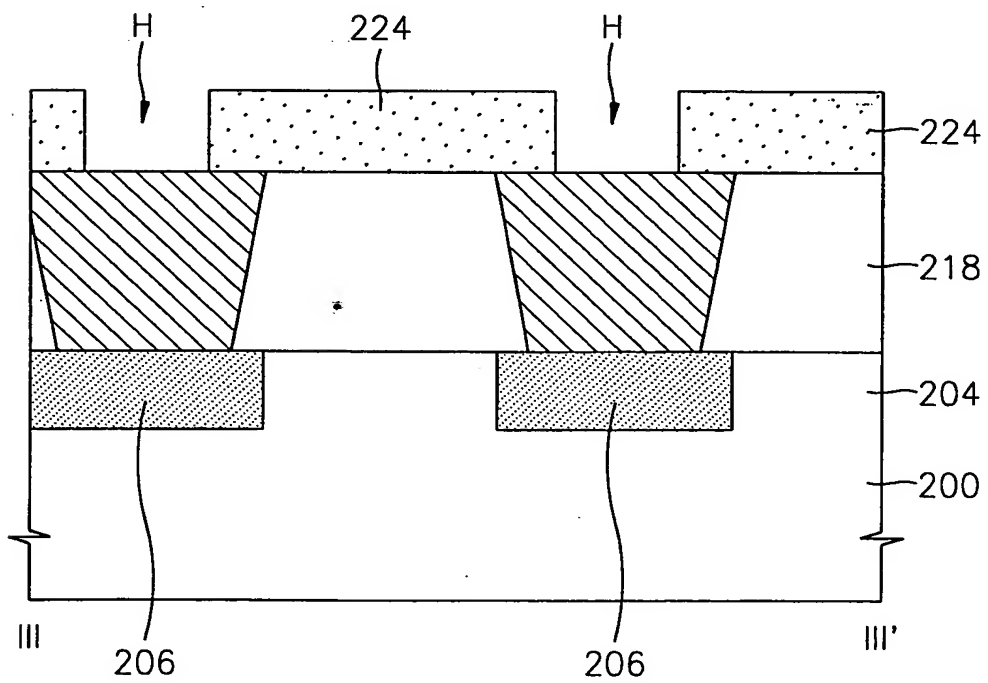
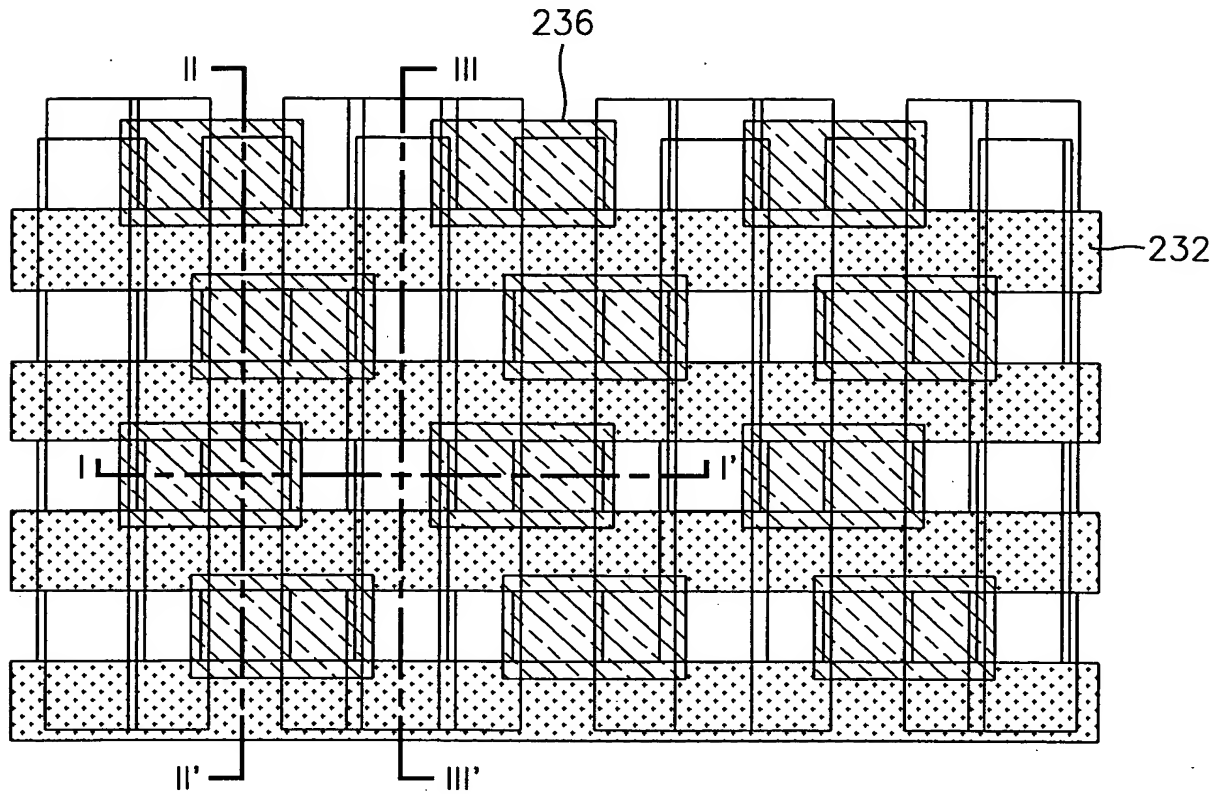


FIG. 7D



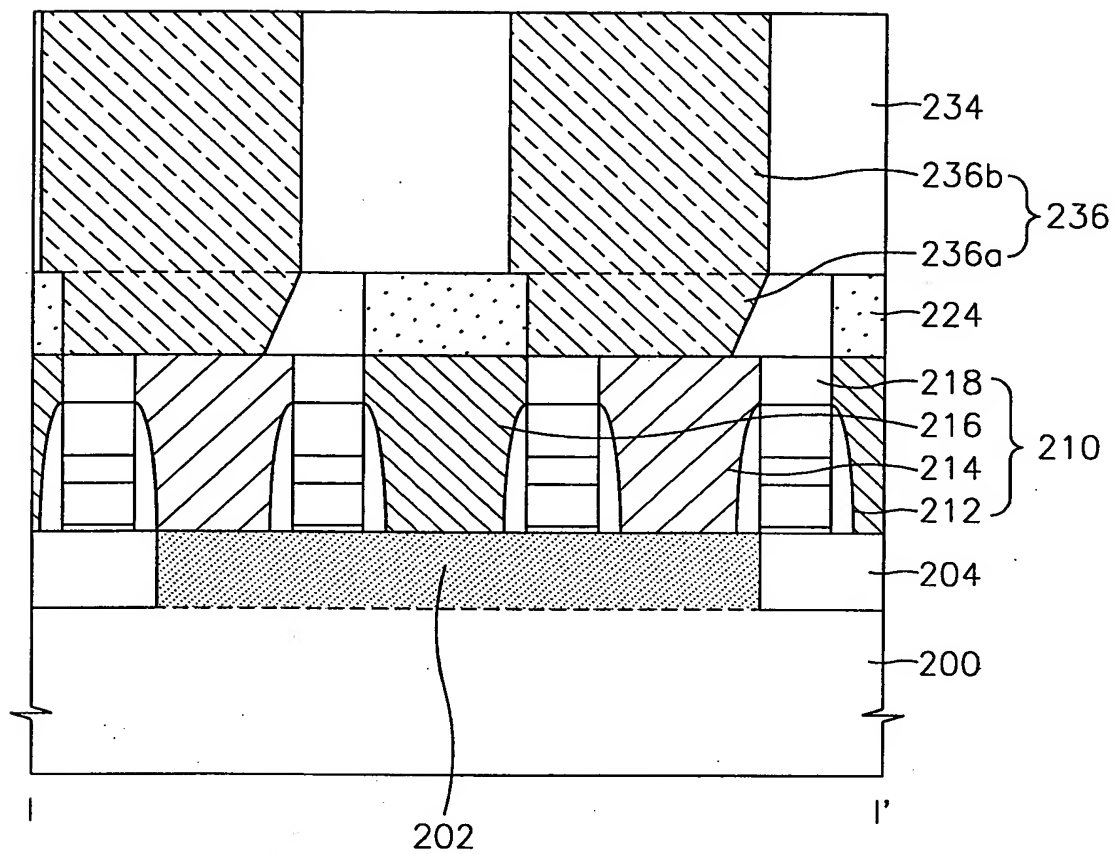
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FIG. 8A



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FIG. 8B



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FIG. 8C

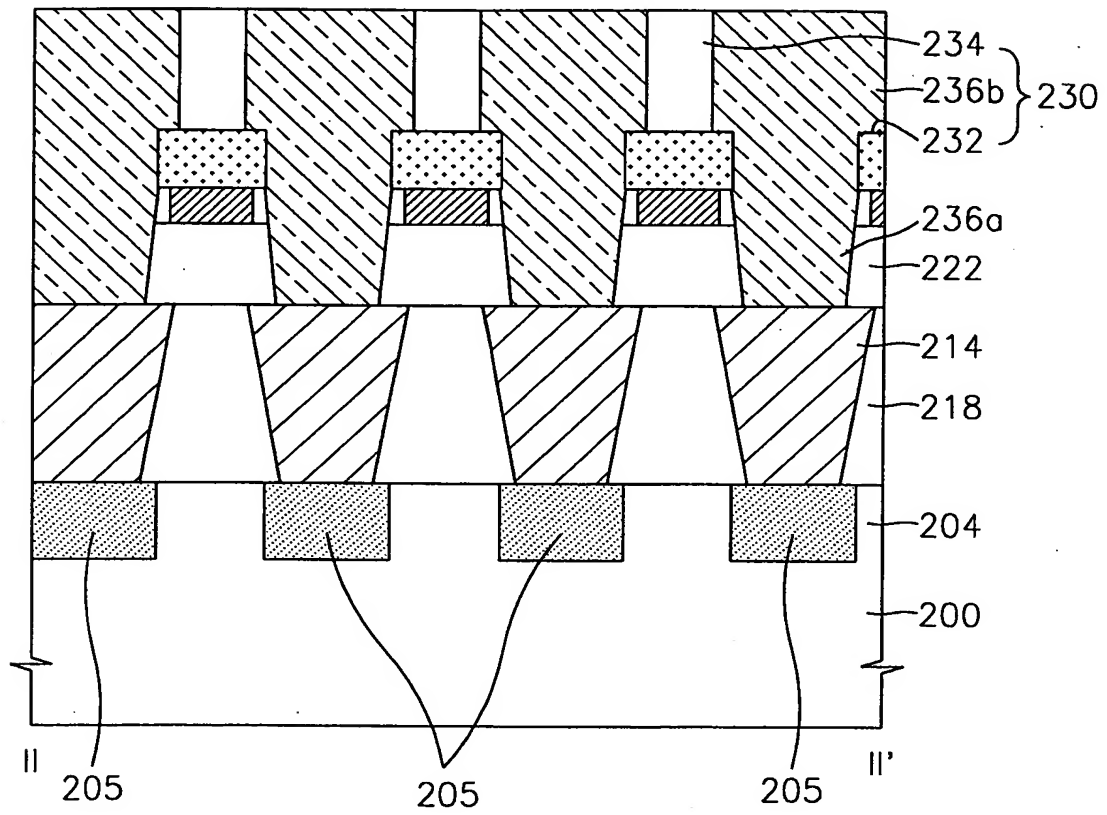
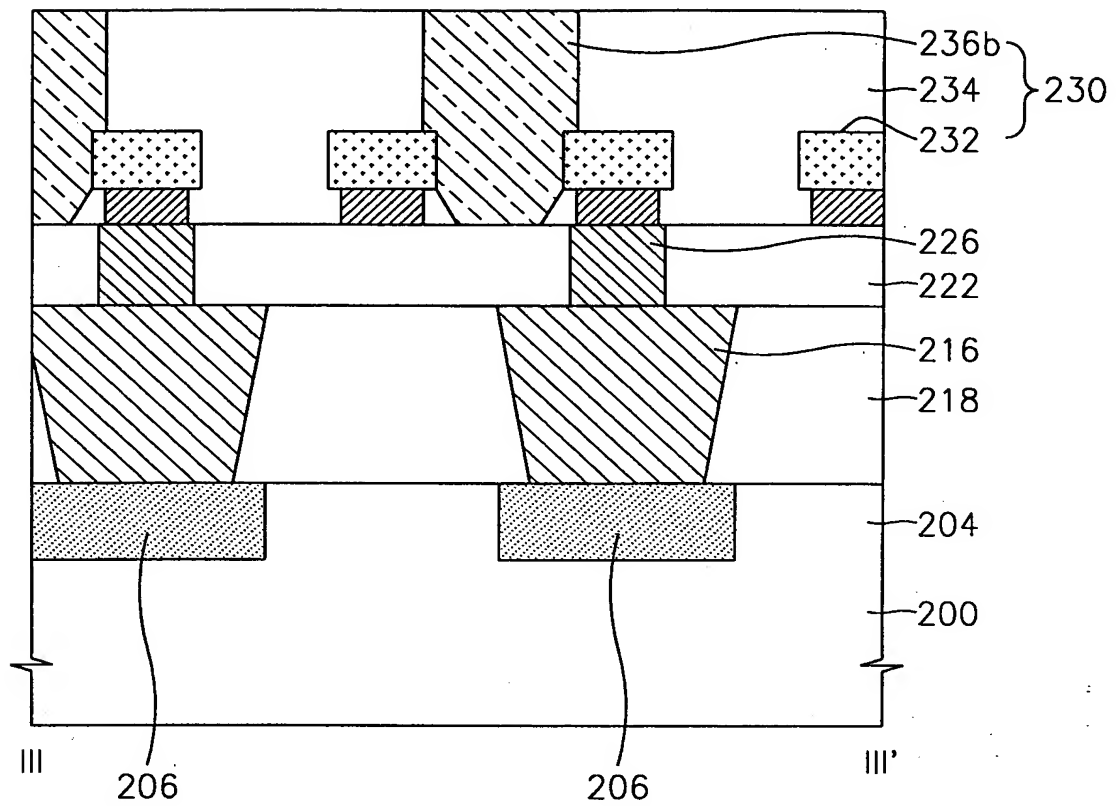
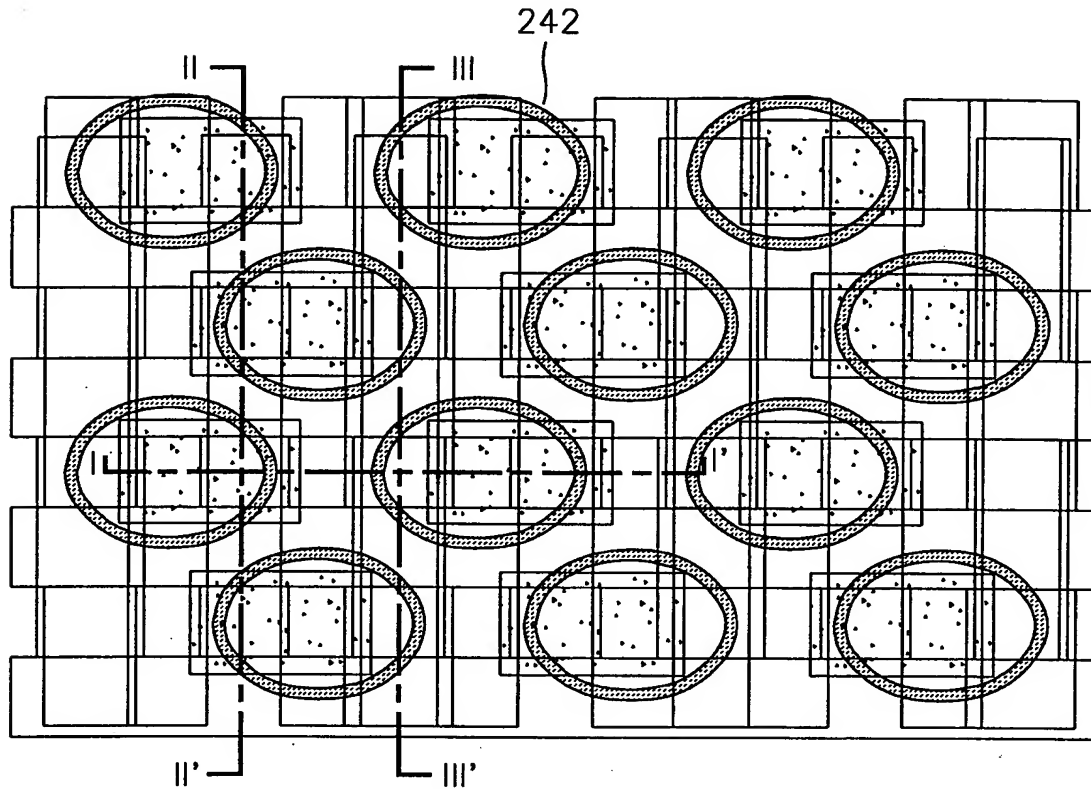


FIG. 8D



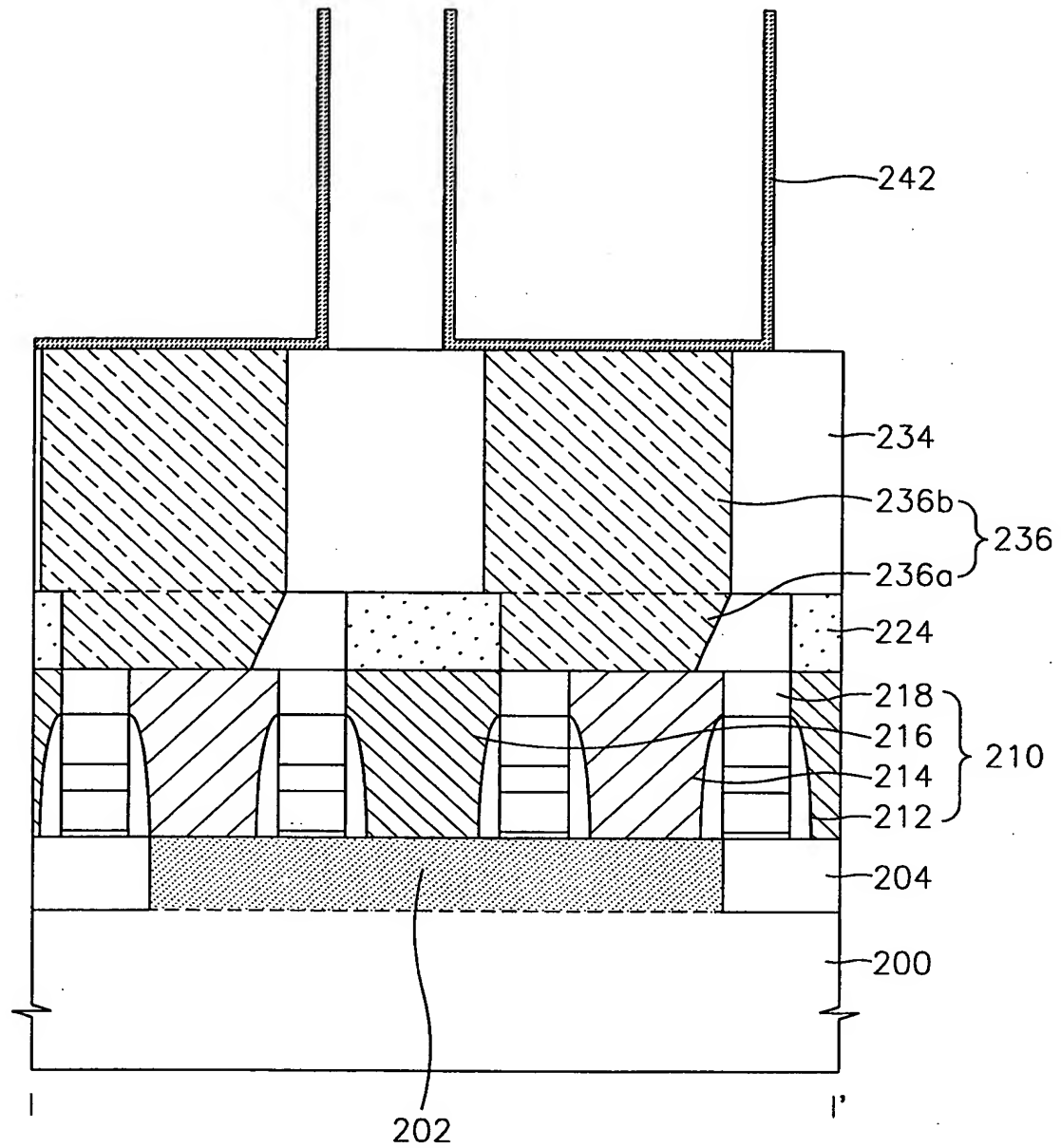
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FIG. 9A



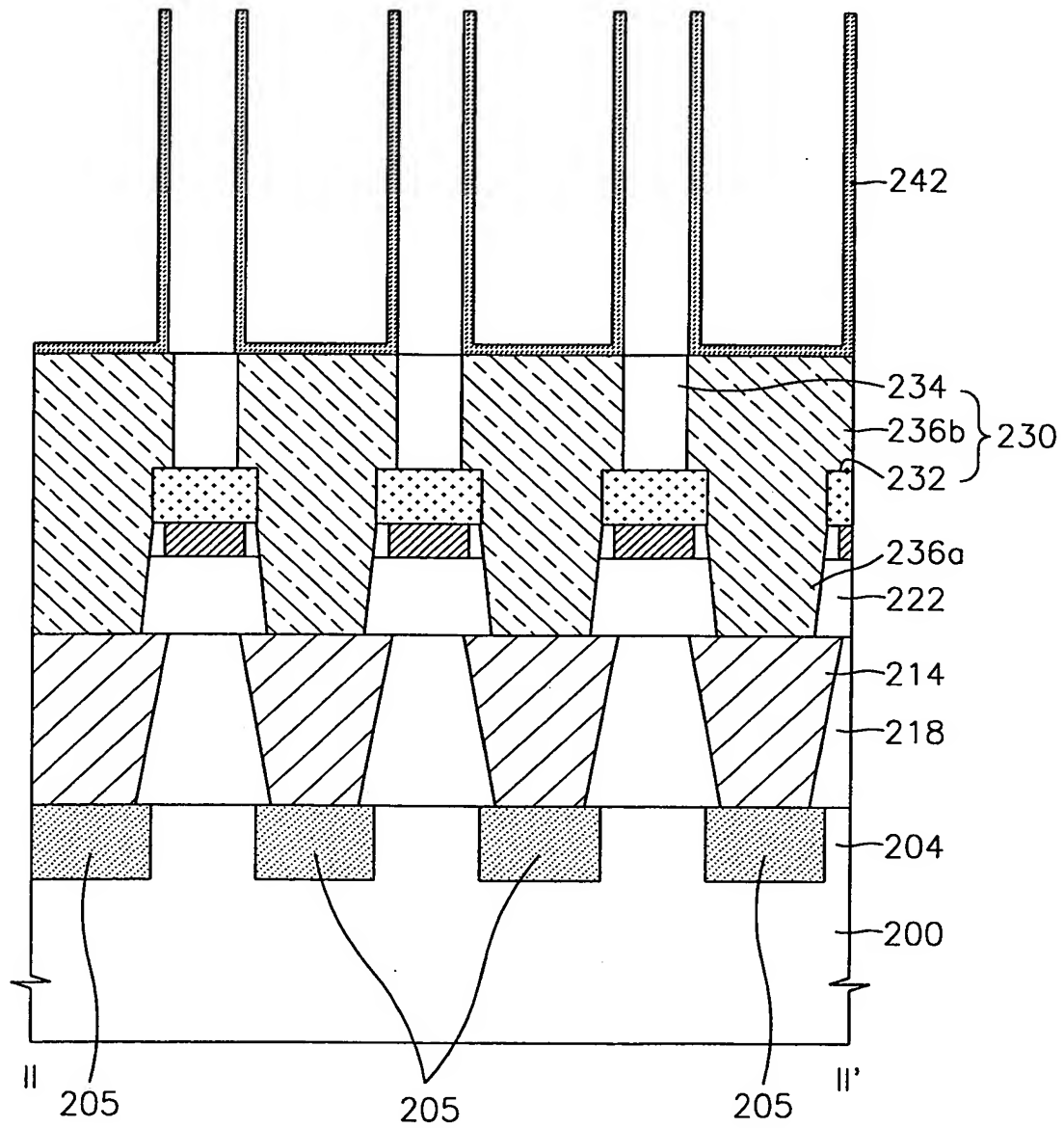
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FIG. 9B



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FIG. 9C





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FIG. 9D

